**Design Record**

**ENEL 453 - Lab 4**

***Group 12***

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RTL of top-level entity:

Chart

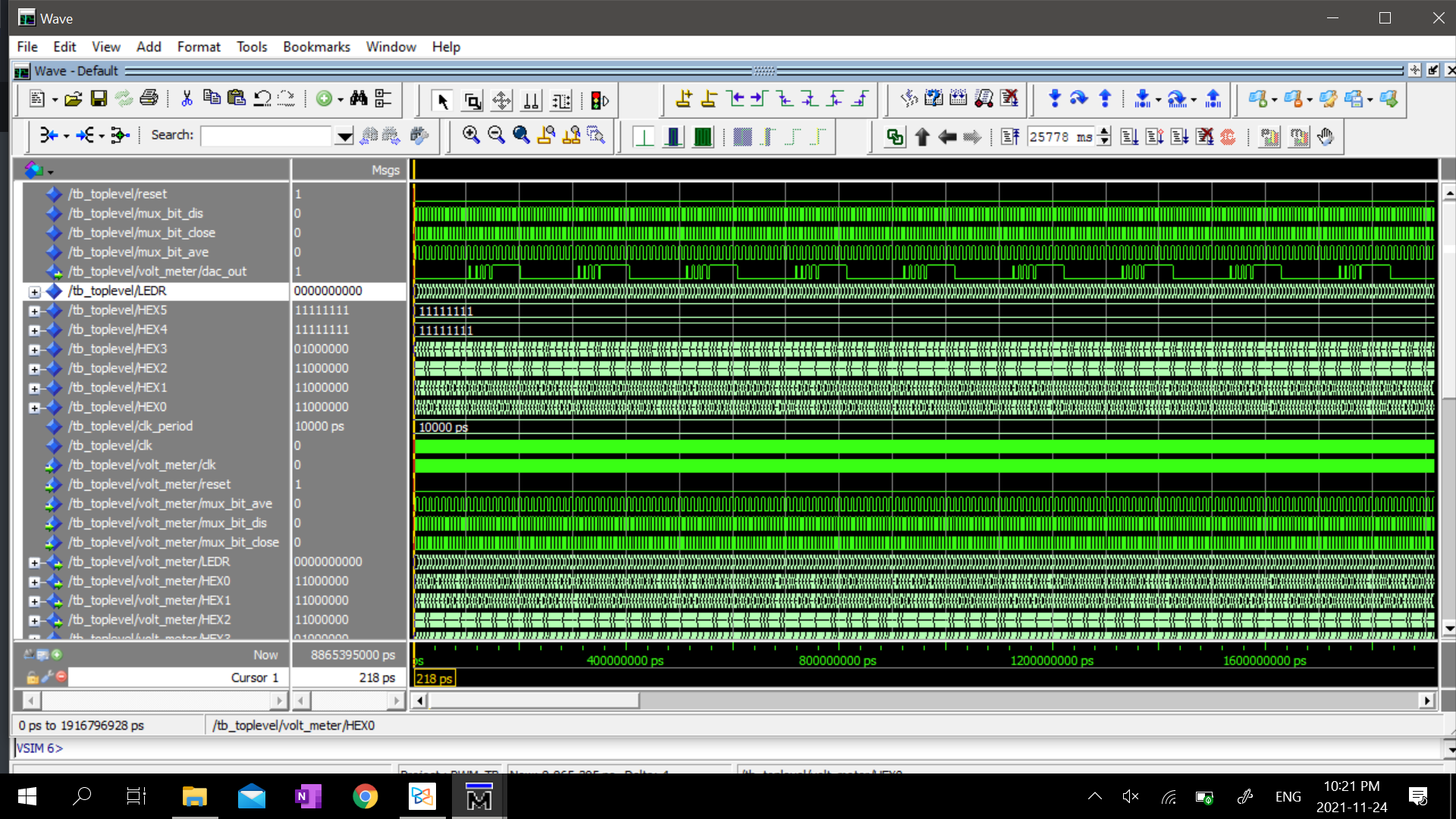
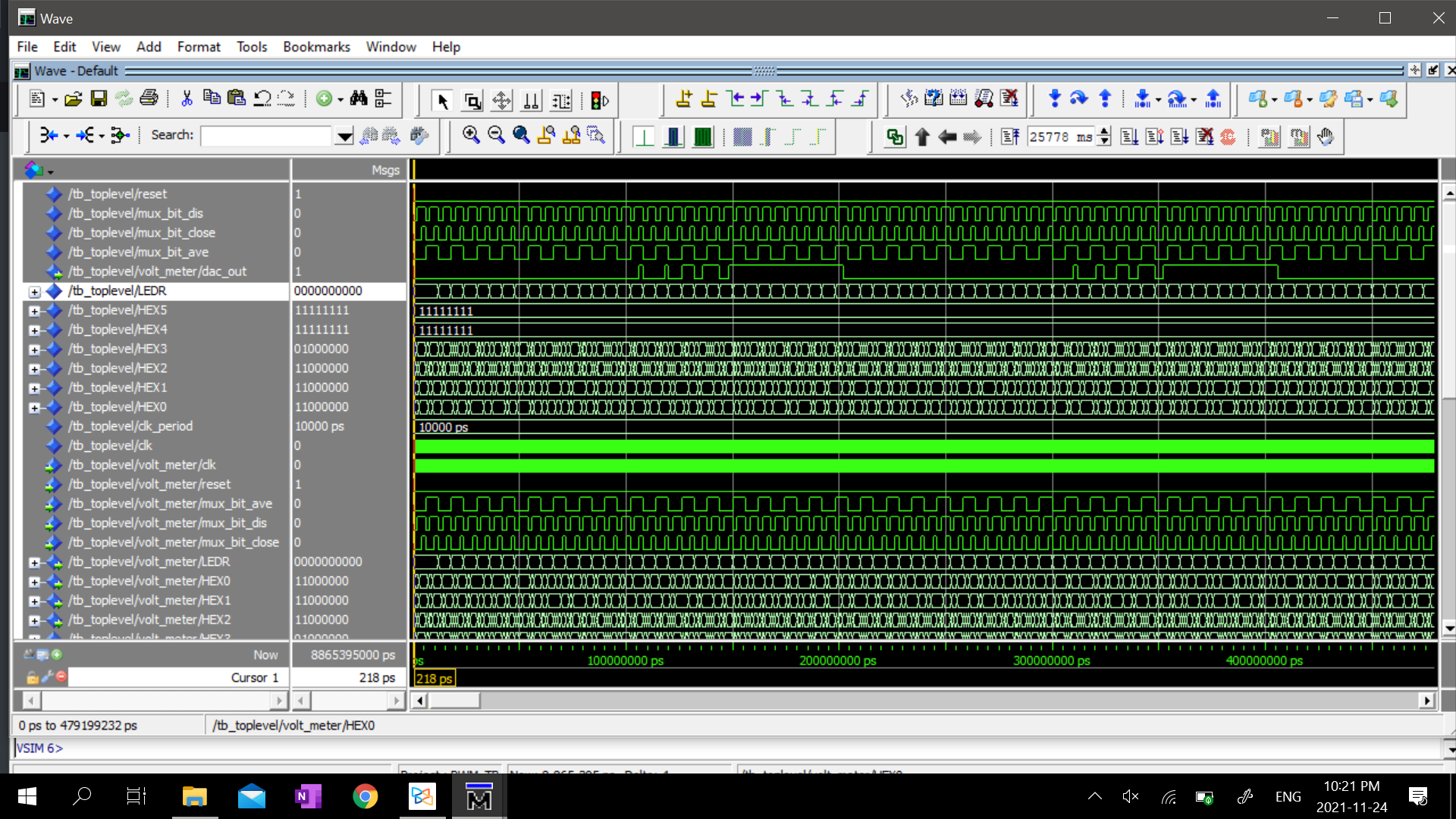
Description automatically generated

Timing Report:

Graphical user interface, text, application

Description automatically generated

Top-Level Testbench:

To stimulate our design, we used the given “test\_ADC” file to generate data; this file simulates a repeated sequence of input voltages to the design. This is why we can see the output “dac\_out” in a repeated sequence, with that sequence made up a square wave of varying frequency. This confirms that the design is successfully outputting a square wave with frequency dependent on voltage (i.e. distance).